

**UNITED STATES DEPARTMENT OF COMMERCE****Patent and Trademark Office**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/207, 972 12/09/98 GARDNER

M 5500-36100

EXAMINER

MMC2/0509

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CONLEY ROSE & TAYON
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WARREN, M	ART UNIT	PAPER NUMBER
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2815
DATE MAILED:

05/09/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)
	09/207,972	GARDNER ET AL.
Examiner	Art Unit	
Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 22 February 2001.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 16-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 16-29 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are objected to by the Examiner.

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) Notice of References Cited (PTO-892)

16) Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____

18) Interview Summary (PTO-413) Paper No(s). _____

19) Notice of Informal Patent Application (PTO-152)

20) Other: _____

DETAILED ACTION

This Office Action is in response to the Amendment filed on February 22, 2001.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 16, 18, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo (US 5,596,214) in view of Ramsby et al. (US 5,972,751).

Endo shows (fig. 3) a semiconductor device comprising a semiconductor substrate (1) and an oxide layer (3) containing nitrogen formed on the substrate (col. 14, lines 57-60). A high dielectric constant film (11), such as the metal oxide BST, is formed on the oxide layer (col. 14, line 64 – col. 15, line 6). BST has a dielectric constant of 510 (col. 12, lines 41-44) which is greater than 5 or 20 as cited in the applicant's claimed invention. A gate conductor (5) is arranged on the high dielectric constant film. Endo does not specifically show that the nitrogen containing oxide layer is a low trap density layer. Ramsby et al. discloses (col. 5, lines 41-45) that nitrogen added to an oxide layer produces a low trap density layer with superior endurance capabilities. Therefore it would have been obvious to one of ordinary skill in the art at time the invention was made that the nitrogen layer of Endo inherently has a low trap

density because Ramsby teaches that adding nitrogen to an oxide layer lowers the trap density and increase the hot carrier lifetime.

Claims 17, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo (US 5,596,214) as applied to claim 16 above, and further in view of Gardner et al. (US 6,015,739).

Endo shows all of the elements of the claims except the silicon nitride layer, the third dielectric layer, and the thickness of the layers being less than 10 angstroms. Gardner et al discloses (col. 5, lines 43-51) a semiconductor device having 5 angstroms of silicon oxide film (120), 10 angstroms of silicon nitride (130), and a third film (140) having a high dielectric constant. The use of silicon nitride provides a barrier layer against impurities and improves reliability of the device. The high dielectric constant third layer provides thick dielectric stack without incurring short channel effects (col. 6, lines 5-26). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the dual gate dielectric layer of Endo by using silicon nitride as the second layer and adding a third high dielectric constant layer as taught by Gardner et al. because such a combination provides a barrier against migrating impurities and prevents short carrier effects.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endo (US 5,596,214) as applied to claim 16 above, and further in view of Chou (US 5,994,734).

Endo shows all of the elements of the claims except the additional gate dielectric and gate conductor formed between the nitrogen-containing oxide and the substrate. Chou shows (figs. 3f, 3g) a semiconductor device having an additional gate conductor layer (23) and a gate dielectric (22) formed between a dielectric stack and the substrate (20) to form a non volatile memory device. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Endo by adding an additional gate conductor and dielectric as taught by Chou to form a non volatile memory device.

Claims 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo (US 5,596,214) in view of Ramsby et al. (US 5,972,751) and Gardner et al. (US 6,015,739).

Endo shows (fig. 3) a semiconductor device comprising a semiconductor substrate (1) and an oxide layer (3) containing nitrogen formed on the substrate (col. 14, lines 57-60). A high dielectric constant film (11), such as the metal oxide BST, is formed on the oxide layer (col. 14, line 64 – col. 15, line 6). BST has a dielectric constant of 510 (col. 12, lines 41-44) which is greater than 5 or 20 as cited in the applicant's claimed invention. A gate conductor (5) is arranged on the high dielectric constant film. Endo does not specifically show that the nitrogen containing oxide layer is a low trap density layer. Ramsby et al. discloses (col. 5, lines 41-45) that nitrogen added to an oxide layer produces a low trap density layer with superior endurance capabilities. Endo and Ramsby show all of the elements of the claims except the silicon

nitride layer, the third dielectric layer, and the thickness of the layers being less than 10 angstroms. Gardner et al discloses (col. 5, lines 43-51) a semiconductor device having 5 angstroms of silicon oxide film (120), 10 angstroms of silicon nitride (130), and a third film (140) having a high dielectric constant. The use of silicon nitride provides a barrier layer against impurities and improves reliability of the device. The high dielectric constant third layer provides thick dielectric stack without incurring short channel effects (col. 6, lines 5-26). Therefore it would have been obvious to one of ordinary skill in the art at time the invention was made that the nitrogen layer of Endo inherently has a low trap density because Ramsby teaches that adding nitrogen to an oxide layer lowers the trap density and increase the hot carrier lifetime. It would have also been obvious to modify the dual gate dielectric layer of Endo by using 10 angstroms of silicon nitride as the second layer and adding a third high dielectric constant layer as taught by Gardner et al. because such a combination provides a barrier against migrating impurities and prevents short carrier effects.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Endo (US 5,596,214) in view of Ramsby et al. (US 5,972,751) as applied to claim 24 above, and further in view of Chou (US 5,994,734).

Endo shows all of the elements of the claims except the additional gate dielectric and gate conductor formed between the nitrogen-containing oxide and the substrate. Chou shows (figs. 3f, 3g) a semiconductor device having an additional gate conductor layer (23) and a gate dielectric (22) formed between a dielectric stack and the substrate

(20) to form a non volatile memory device. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Endo by adding an additional gate conductor and dielectric as taught by Chou to form a non volatile memory device.

Response to Arguments

Applicant's arguments with respect to claims 16-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wristers et al. (US 5,591,681) and Kusunoki et al. (US 5,648,284) also disclose nitrogen containing oxide layers that have low trap densities.

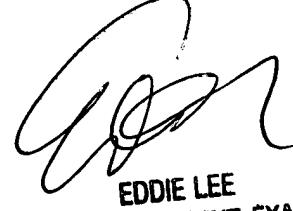
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW

May 7, 2001



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800